Claims

We claim:

1. A radio-frequency (RF) apparatus, comprising:

receiver analog circuitry configured to produce a at least one digital receive signal from an analog radio-frequency signal, the receiver analog circuitry having a plurality of signal lines, the signal lines being configurable by a control signal; and

receiver digital circuitry configured to accept the at least one digital receive signal from the receiver analog circuitry, the receiver digital circuitry having a plurality of signal lines coupled to the signal lines of the analog receiver circuitry, the signal lines of the digital receiver circuitry being configurable by the control signal.

2. The RF apparatus of claim 1, in which the signal lines of the receiver analog circuitry and the signal lines of the receiver digital circuitry are configured as a data and clock signal interface when the control signal is in a first state.

3. The RF apparatus of claim 2, in which the signal lines of the receiver analog circuitry and the signal lines of the receiver digital circuitry are configured as a serial interface when the control signal is in a second state.

4. The RF apparatus of claim 3, in which the serial interface includes a plurality of data signals and a plurality of control signals.

5. The RF apparatus of claim 4, in which the plurality of control signals includes a clock signal, wherein the clock signal is a band-limited current signal.

6. The RF apparatus of claim 5, in which the plurality of control signals includes a serial interface enable signal, wherein the serial interface enable signal is a band-limited current signal.

7. The RF apparatus of claim 6, in which the plurality of data signals includes a serial data-in signal, wherein the serial data-in signals is a band-limited current signal.

8. The RF apparatus of claim 7, in which the plurality of data signals includes a serial data-out signal, wherein the serial data-out signal is a band-limited current signal.

9. The RF apparatus of claim 8, in which the receiver analog circuitry resides within a first integrated circuit device and the receiver digital circuitry resides within a second integrated circuit device.

10. The RF apparatus of claim 3, in which the data and clock interface includes a data signal and a clock signal.

11. The RF apparatus of claim 10, in which the data signal is a band-limited differential current signal.

12. The RF apparatus of claim 11, in which the clock signal is a band-limited differential signal.

13. The RF apparatus of claim 12, in which the receiver analog circuitry resides within a first integrated circuit device and the receiver digital circuitry resides within a second integrated circuit device.

14. A radio-frequency (RF) transceiver, comprising:

a first integrated-circuit device that includes receiver analog circuitry configured to produce a at least one digital receive signal from an analog radio-frequency signal, the receiver analog circuitry having a plurality of signal lines that are configurable by a control signal; and

a second integrated-circuit device that includes receiver digital circuitry configured to accept the at least one digital receive signal from the receiver analog circuitry, the receiver digital circuitry having a plurality of signal lines that are configurable by the control signal,

wherein the signal lines of the analog receiver circuitry are coupled to the signal lines of the receiver digital circuitry.

15. The transceiver of claim 14, in which the signal lines of the receiver analog circuitry and the signal lines of the receiver digital circuitry are configured as a data and clock signal interface when the control signal is in a first state.

16. The transceiver of claim 15, in which the signal lines of the receiver analog circuitry and the signal lines of the receiver digital circuitry are configured as a serial interface when the control signal is in a second state.

17. The transceiver of claim 16, in which the serial interface includes a plurality of data signals and a plurality of control signals.

18. The transceiver of claim 17, in which the plurality of control signals includes a clock signal and a serial interface enable signal.

19. The transceiver of claim 18, in which the plurality of data signals includes a serial data-in signal and a serial data-out signal.

20. The transceiver of claim 19, in which the receiver digital circuitry includes a plurality of signal driver circuitries configured to provide the plurality of data signals and the plurality of control signals of the serial interface to the receiver analog circuitry when the control signal is in the second state.

21. The transceiver of claim 20, in which the receiver analog circuitry includes a plurality of data receiver circuitries configured to accept the plurality of data signals and the plurality of control signals from the receiver digital circuitry when the control signal is in the second state.

22. The transceiver of claim 21, in which receiver digital circuitry includes interface controller circuitry configured to cause serial data-out from the receiver analog circuitry to be received within the receiver digital circuitry, the interface controller circuitry further configured to cause serial data-out within the receiver digital circuitry to be selectively provided to baseband processor circuitry coupled to the second integrated circuit.

23. The transceiver of claim 22, in which the plurality of data signals and the plurality of control signals comprise band-limited current signals.

24. The transceiver of claim 16, in which the data and clock interface includes a data signal and a clock signal.

25. The transceiver of claim 24, in which the receiver digital circuitry includes clock driver circuitry configured to provide the clock signal when the control signal is in the first state.

26. The transceiver of claim 25, in which the receiver analog circuitry includes clock receiver circuitry configured to accept the clock signal from the receiver digital circuitry when the control signal is in the first state.

27. The transceiver of claim 26, in which the receiver analog circuitry includes data driver circuitry configured to provide the data signal when the control signal is in the first state.

28. The transceiver of claim 27, in which the receiver digital circuitry includes at least one data receiver circuitry configured to accept the data signal from the receiver analog circuitry when the control signal is in the first state.

29. The transceiver of claim 28, in which the clock signal comprises a band-limited differential current signal.

30. The transceiver of claim 29, in which the data signal comprises a band-limited differential current signal.

31. The transceiver of claim 30, in which the receiver analog circuitry includes multiplexer circuitry configured to provide the data signal to the data driver circuitry in response to a data transfer clock.

32. The transceiver of claim 31, in which the multiplexer circuitry is further configured to accept a pair of output signals from an analog-to-digital converter (ADC) circuitry within the receiver analog circuitry, and to provide as the data signal each of the output signals on alternating transitions of the data transfer clock.

33. The transceiver of claim 32, in which the receiver analog circuitry derives the data transfer clock from the clock signal provided by the receiver digital circuitry.

34. A method of interfacing receiver digital circuitry and receiver analog circuitry within a radio-frequency (RF) apparatus, comprising:

providing receiver analog circuitry having a plurality of signal lines that are configurable by a control signal;

utilizing the receiver analog circuitry to produce at least one digital receive signal from an analog radio-frequency signal;

providing receiver digital circuitry having a plurality of signal lines that are configurable by the control signal and are coupled to the signal lines of the receiver analog circuitry; and

accepting in the receiver digital circuitry the at least one digital receive signal from the receiver analog circuitry.

35. The method of claim 34, which further comprises configuring the signal lines of the receiver analog circuitry and the signal lines of the receiver digital circuitry as a data and clock signal interface when the control signal is in a first state.

36. The method of claim 35, which further comprises configuring the signal lines of the receiver analog circuitry and the signal lines of the receiver digital circuitry as a serial interface when the control signal is in a second state.

37. The method of claim 36, which further comprises configuring the serial interface to include a plurality of data signals and a plurality of control signals.

38. The method of claim 37, which further includes providing a clock signal in the plurality of control signals, wherein the clock signal is a band-limited current signal.

39. The method of claim 38, which further comprises providing a serial interface enable signal in the plurality of control signals, wherein the serial interface enable signal is a band-limited current signal.

40. The method of claim 39, which further includes providing a serial data-in signal in the plurality of data signals, wherein the serial data-in signal is a band-limited current signal.

41. The method of claim 40, which further comprises providing a serial data-out signal in the plurality of data signals, wherein the serial data-out signal is a band-limited current signal.

42. The method of claim 41, further comprising:

providing the receiver analog circuitry within a first integrated circuit device; and

providing the receiver digital circuitry within a second integrated circuit device.

43. The method of claim 36, which further comprises providing a data signal and a clock signal in the data and clock interface.

44. The method of claim 43, which further comprises providing the data signal as a band-limited differential current signal.

45. The method of claim 44, which further comprises providing the clock signal as a band-limited differential current signal.

46. The method of claim 45, further comprising:

providing the receiver analog circuitry within a first integrated circuit device; and

providing the receiver digital circuitry within a second integrated circuit device.

47. A method of interfacing receiver digital circuitry and receiver analog circuitry within a radio-frequency (RF) transceiver, comprising:

providing in a first integrated-circuit device a receiver analog circuitry having a plurality of signal lines that are configurable by a control signal;

utilizing the receiver analog circuitry to produce at least one digital receive signal from an analog radio-frequency signal;

providing in a second integrated-circuit device a receiver digital circuitry having a plurality of signal lines that are configurable by the control signal and are coupled to the signal lines of the receiver analog circuitry; and

accepting in the receiver digital circuitry the at least one digital receive signal from the receiver analog circuitry.

48. The method of claim 47, which further comprises configuring the signal lines of the receiver analog circuitry and the signal lines of the receiver digital circuitry as a data and clock signal interface when the control signal is in a first state.

49. The method of claim 48, which further comprises configuring the signal lines of the receiver analog circuitry and the signal lines of the receiver digital circuitry as a serial interface when the control signal is in a second state.

50. The method of claim 49, which further comprises configuring the serial interface to include a plurality of data signals and a plurality of control signals.

51. The method of claim 50, which further comprises providing in the plurality of control signals a clock signal and a serial interface enable signal.

52. The method of claim 51, which further comprises providing in the plurality of data signals a serial data-in signal and a serial data-out signal.

53. The method of claim 52, which further comprises providing a plurality of signal driver circuitries within the receiver digital circuitry, wherein the plurality of signal driver circuitries configured to provide the plurality of data signals and the plurality of control signals of the serial interface to the receiver analog circuitry when the control signal is in the second state.

54. The method of claim 53, which further comprises providing a plurality of data receiver circuitries within the receiver analog circuitry, wherein the plurality of data receiver circuitries are configured to accept the plurality of data signals and the plurality of control signals from the receiver digital circuitry when the control signal is in the second state.

55. The method of claim 54, which further comprises providing interface controller circuitry within the receiver digital circuitry, wherein the interface controller circuitry is configured to cause serial data-out from the receiver analog circuitry to be received within the receiver digital circuitry, and wherein the interface controller circuitry is further configured to cause serial data-out within the receiver digital circuitry to be selectively provided to baseband processor circuitry coupled to the second integrated circuit.

56. The transceiver of claim 55, which further comprises providing the plurality of data signals and the plurality of control signals as band-limited current signals.

57. The method of claim 49, which further comprises configuring the data and clock interface to include a data signal and a clock signal.

58. The method of claim 57, which further comprises providing clock driver circuitry within the receiver digital circuitry, wherein the clock driver circuitry is configured to provide the clock signal when the control signal is in the first state.

59. The method of claim 58, which further comprises providing clock receiver circuitry within the receiver analog circuitry, wherein the clock receiver circuitry is configured to accept the clock signal from the receiver digital circuitry when the control signal is in the first state.

60. The method of claim 59, which further comprises providing data driver circuitry within the receiver analog circuitry, wherein the data driver circuitry is configured to provide the data signal when the control signal is in the first state.

61. The method of claim 60, which further comprises providing data receiver circuitry within the receiver digital circuitry, wherein the data receiver circuitry is configured to accept the data signal from the receiver analog circuitry when the control signal is in the first state.

62. The method of claim 61, which further comprises providing the clock signal as a band-limited differential current signal.

63. The method of claim 62, which further comprises providing the data signal as a band-limited differential current signal.

64. The method of claim 63, which further comprises providing multiplexer circuitry within the receiver analog circuitry, wherein the multiplexer circuitry is configured to provide the data signal to the data driver circuitry in response to a data transfer clock.

65. The method of claim 64, which further comprises:

providing within the receiver analog circuitry an analog-to-digital converter circuitry (ADC) configured to provide a pair of output signals; and

using the multiplexer circuitry to provide as the data signal each of the output signals of the analog-to-digital converter circuitry on alternating transitions of the data transfer clock.

66. The method of claim 65, which further comprises deriving within the receiver analog circuitry the data transfer clock from the clock signal provided by the receiver digital circuitry.